

# ***Scrubbing and In-Orbit Re-Configuration Options Using the XQRKU060 .***

***Dr. Rajan Bedi  
President of Spacechips LLC***

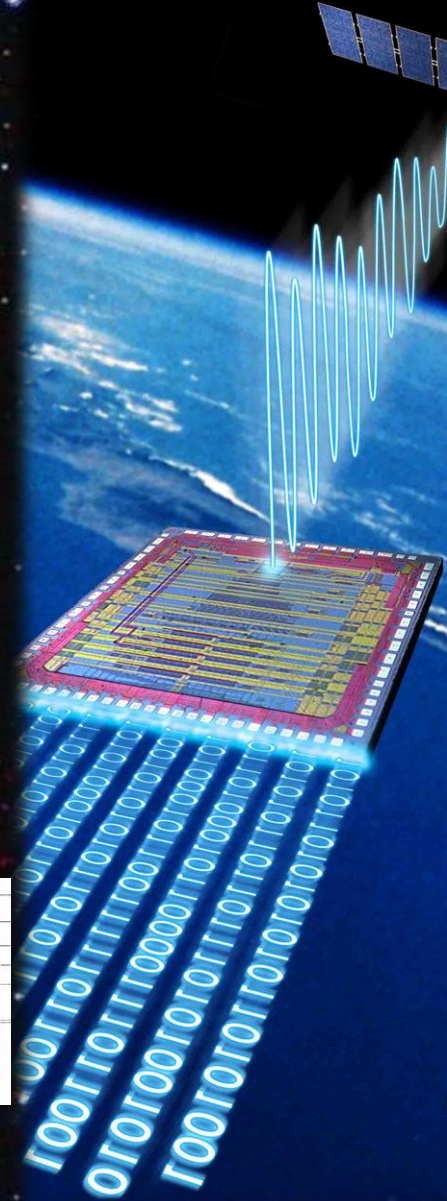
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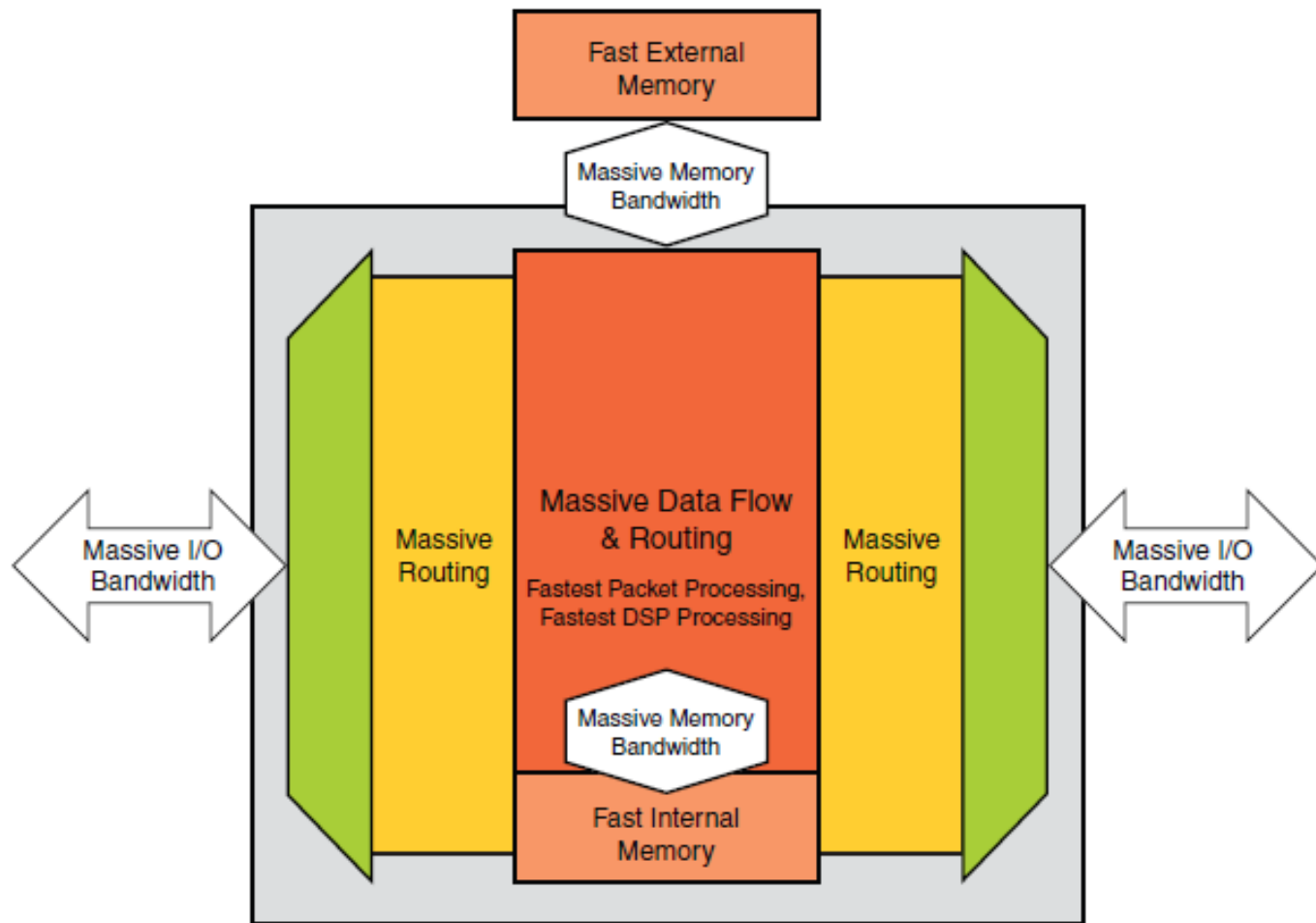
***Winner of Start-Up Company of 2017 & High-Reliability Product of 2016, 17 & 18***



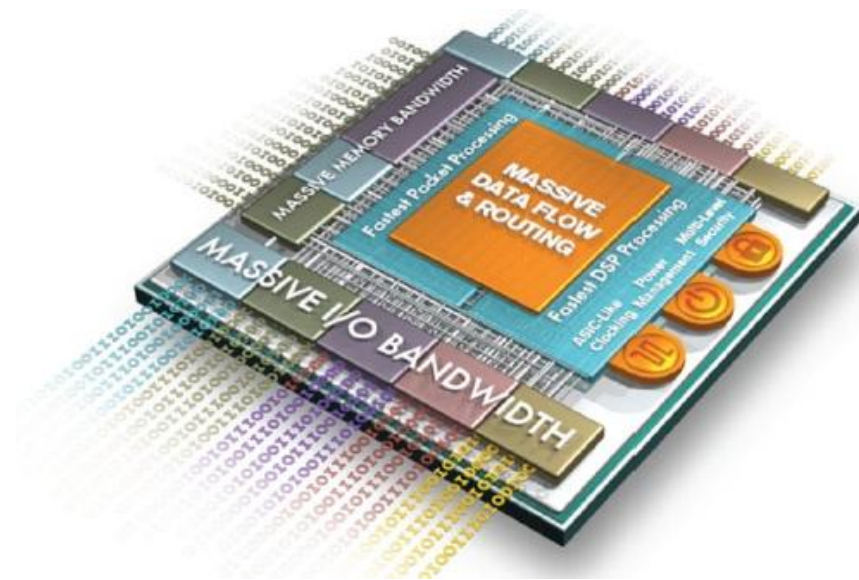
# *Agenda*

- *Introduction to the XQRKU060 FPGA*
- *Introduction to FPGA Scrubbing*
- *Scrubbing Options for the XQRKU060*
  - *Internal using the SEM IP*
  - *External Blind Scrubbing with Readback/Writeback*
  - *External Blind Scrubbing without Readback*
- *In-Orbit Re-Configuration Options for the XQRKU060*
- *Conclusions*
- *Q & A*

# *High-Performance Systems Require Massive Bandwidth*



# On-Board Processing Advantages of the XQRKU060



- *Massive data flow*
- *Highly optimized critical paths and built-in high-speed memory, cascading to remove bottlenecks in DSP and packet processing*
- *Enhanced DSP slices*
- *Massive I/O and memory bandwidth*
- *Multi-region ASIC-like clocking, delivering low-power clock networks with extremely low clock skew and high-performance scalability*
- *Power management with significant static and dynamic-power gating across a wide range of functional elements, yielding significant power savings*
- *Massive routing capacity*



	XQRV4QV	XQRV5QV	XQRKU060
<b>Radiation Hardness</b>	Tolerant	Hard	Tolerant
<b>Process (nm)</b>	90	65	20
<b>Memory (Mb)</b>	4.1 to 9.9	12.3	38
<b>System Logic Cells (k)</b>	55 to 200	131	726
<b>CLB Flip-Flops (k)</b>	49.1 to 178.1	81.9	663
<b>CLB LUTs (k)</b>	49.1 to 178.1	81.9	331
<b>MGTs</b>	None	18 at 3.125 Gbps	32 at 12.5 Gbps
<b>User I/O</b>	640 to 960	836	620
<b>DSP Slices</b>	32 to 192	320	2,760



# SEM IP

## Soft Error Mitigation Controller v4.1

### *LogiCORE IP Product Guide*

Vivado Design Suite

PG036 April 4, 2018

$$DetectionLatency = 22ms \cdot \left[ \frac{200MHz}{90MHz} \right] = 48.889ms$$

$$CorrectionLatency = 41\mu s \cdot \left[ \frac{200MHz}{90MHz} \right] = 0.091ms$$

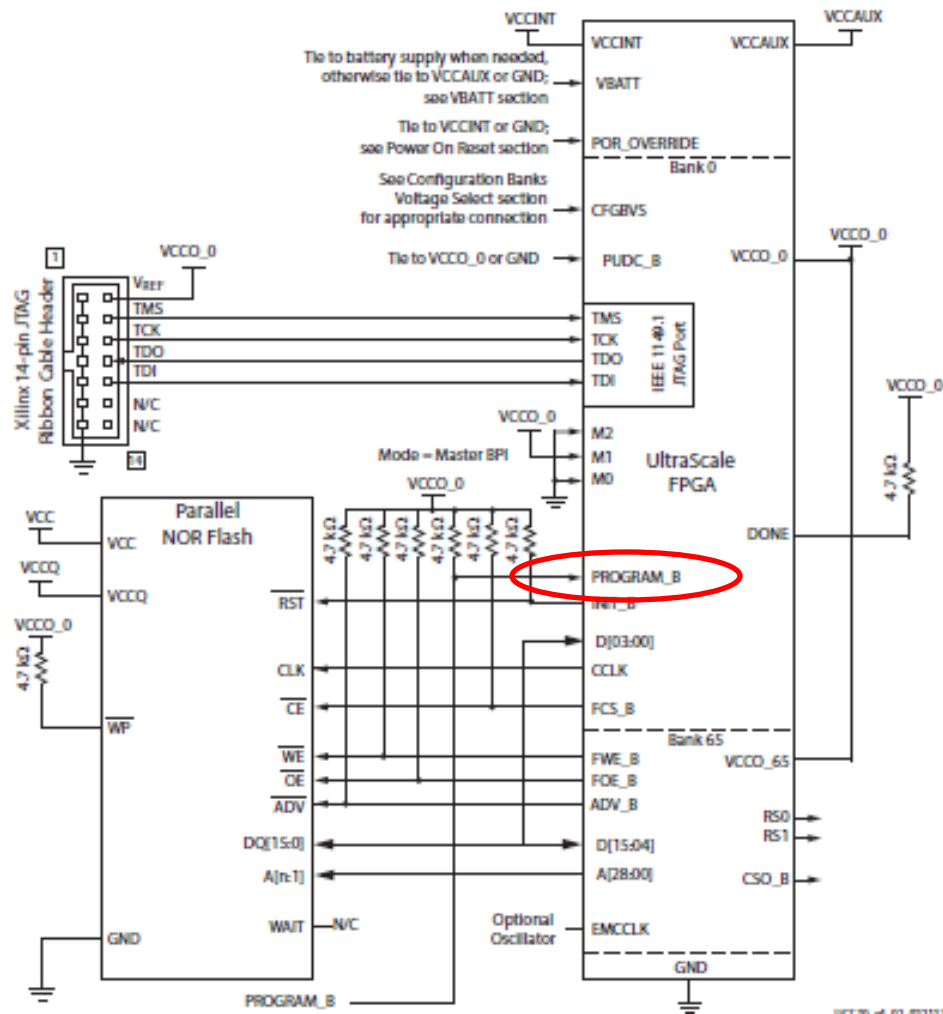
$$ClassificationLatency = 5\mu s \cdot \left[ \frac{200MHz}{90MHz} \right] = 0.011ms$$

$$MitigationLatency = 48.889ms + 0.091ms + 0.011ms = 48.991ms$$



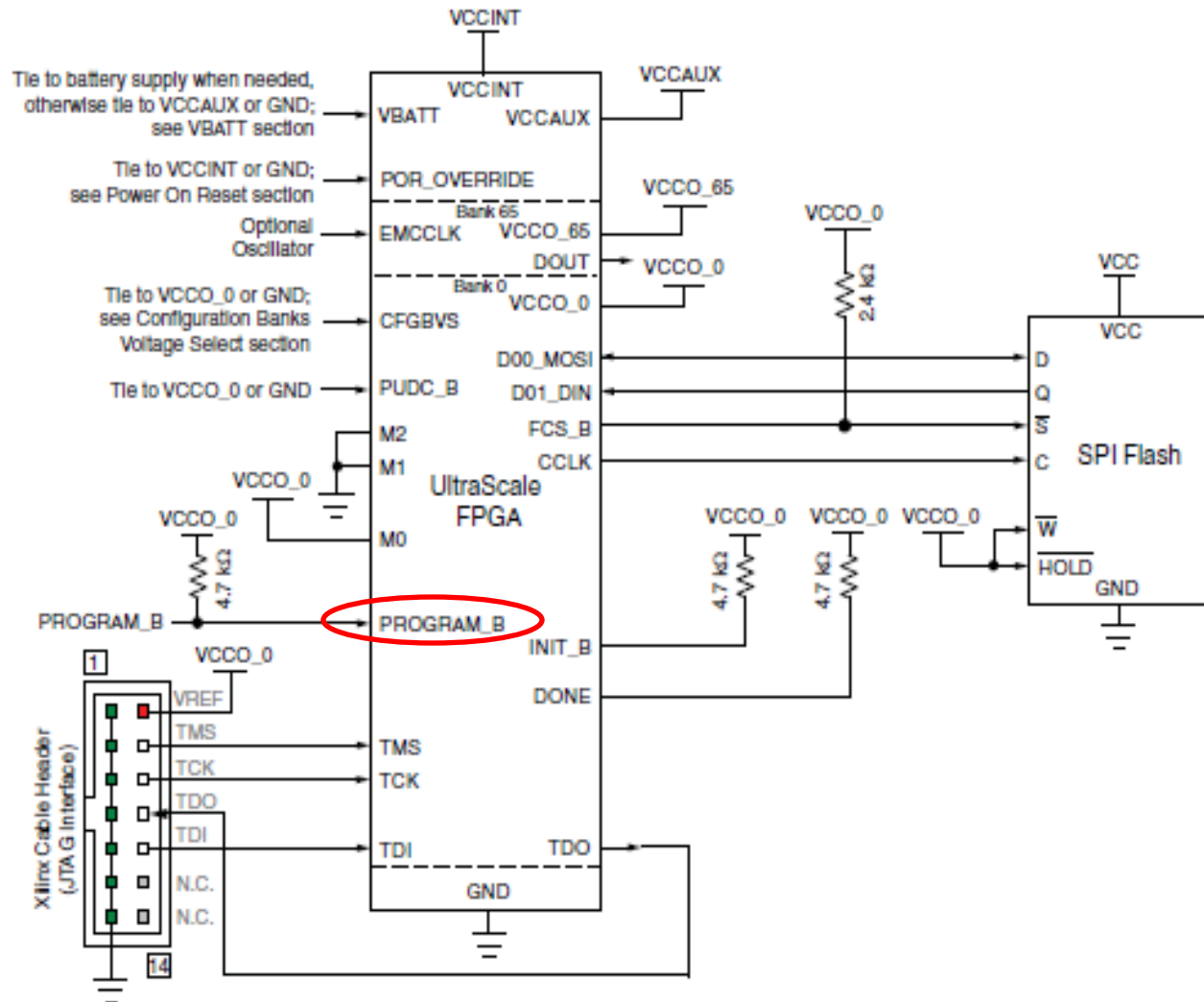
*SEM IP requires 425 LUTs, 490 flip-flops, 59 I/O, 4 RAMB36 blocks and one DSP48 core when implemented on the XQRKU060. An arbiter is also available to share the ICAP between the SEM IP and other functions.*

# External Blind Scrubbing Master BPI Configuration Mode

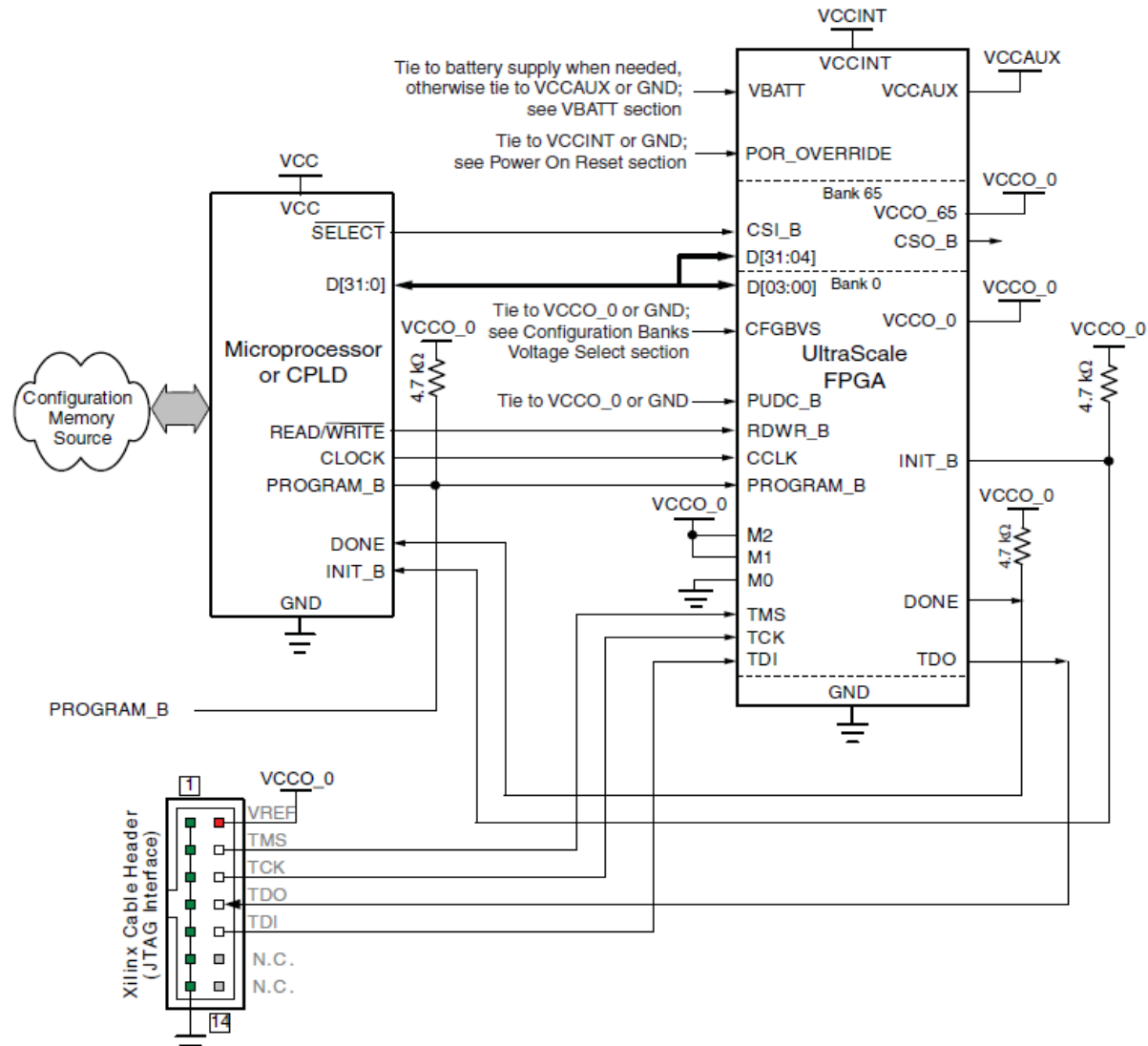




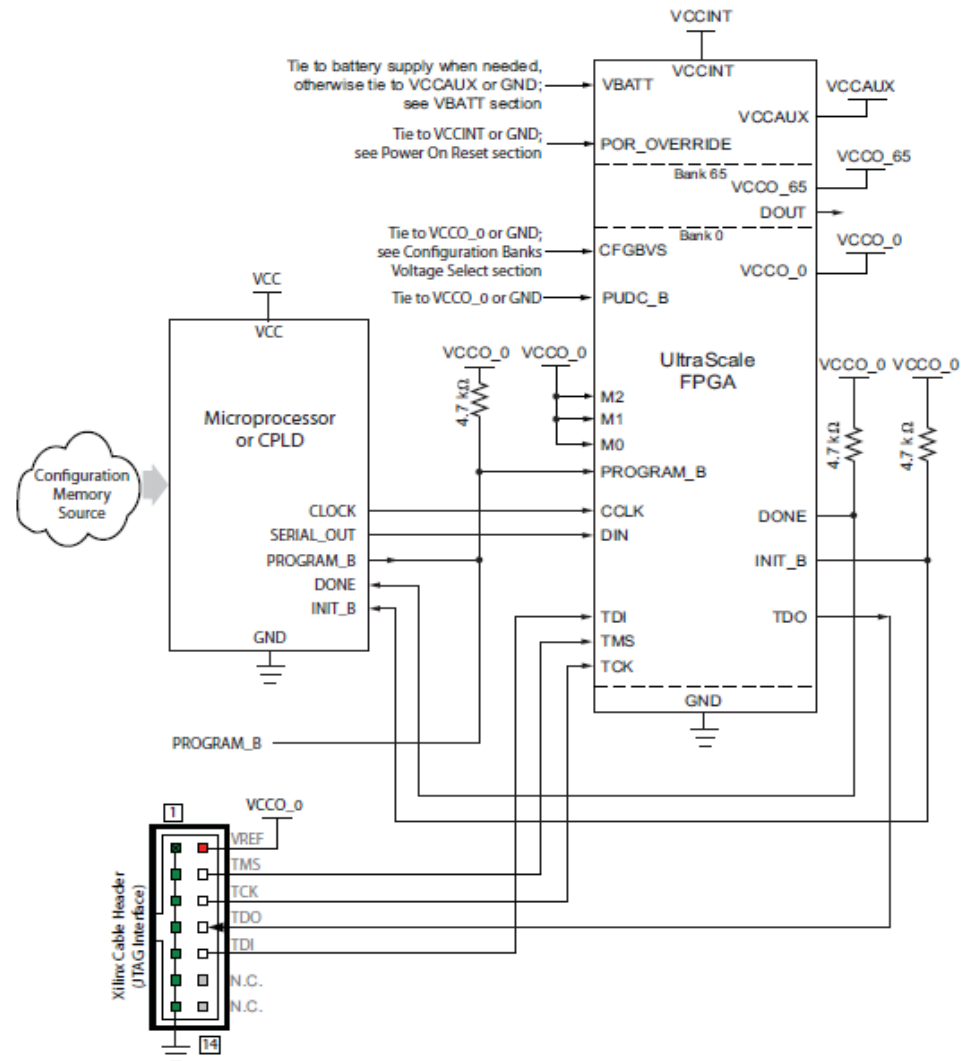
# *External Blind Scrubbing Master Serial Configuration Mode*



# Slave SelectMap Configuration Mode



# Slave Serial Configuration Mode



# *Clock rates, data widths and bandwidths for XQRKU060 configuration ports*

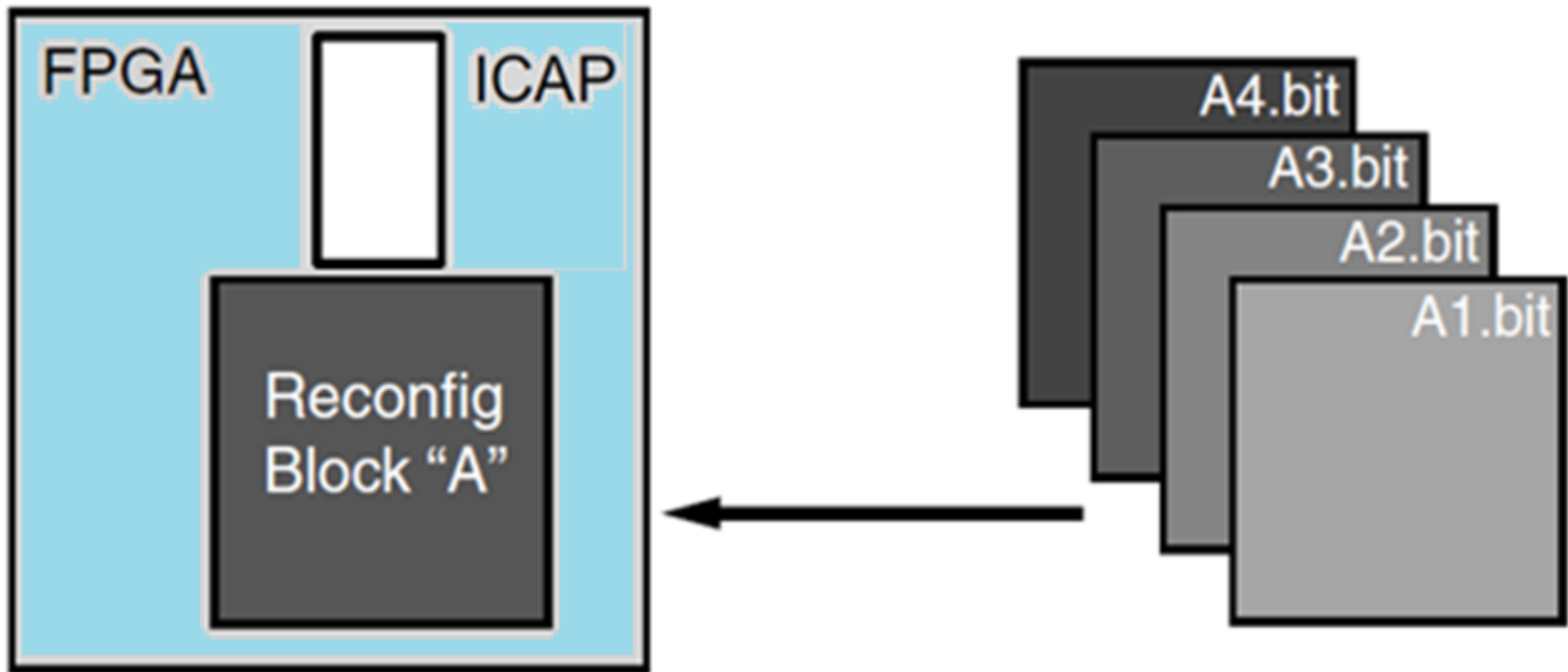
Configuration Mode	Max Clock Rate	Data Width	Maximum Bandwidth
ICAP/MCAP	200 MHz	32 bit	6.4 Gb/s
ICAP/MCAP (SSI)*	125 MHz	32 bit	4.0 Gb/s
SelectMAP	125 MHz	32 bit	4.0 Gb/s
Serial Mode	150 MHz	1 bit	150 Mb/s
Serial (SSI Devices)	100 MHz	1 bit	100 Mb/s
JTAG	50 MHz	1 bit	50 Mb/s
JTAG (SSI Devices)	20 MHz	1 bit	20 Mb/s

# V5QV SEFIs

SEFI	Name	Symptoms	Detection	Action
Design Intrusive <sup>(1)</sup>	Power on reset (POR)	DONE transitions Low Application function cease Decreased V <sub>CCINT</sub> current Large readback error count	Monitor DONE bit in status register Monitor DONE pin	Pulse PROGRAM_B
Design Intrusive <sup>(1)</sup>	Global signal (GSIG)	Design functions cease	Monitor CTL0 and status register for GHIGH, GTS, or GWE going to logic 0	Pulse PROGRAM_B
Visibility Loss <sup>(2)</sup>	Frame Address Register (FAR)	FAR incrementing uncontrollably SelectMAP port is functional	Readback FAR value, compare against known FAR value for differences	Steps: Rewrite FAR value Pulse PROGRAM_B
Visibility Loss <sup>(2)</sup>	SelectMAP (SMAP) or JTAG	Readback all 1s or 0s from the SelectMAP port BUSY signal never returns Low from readback in excess of 16 CCLK cycles Loss of read or write capabilities	Monitor readback data Monitor BUSY signal or configuration registers	Pulse PROGRAM_B
Fake <sup>(3)</sup>	Shutdown (SU)	DONE transitions Low Design continues to run	Monitor DONE signal Monitor user design functionality	Steps: Issue START command Pulse PROGRAM_B

1. The user design does not function as intended and needs to be dealt with immediately upon detection.
2. The SelectMAP interface or configuration circuitry within the Virtex-5QV FPGA is affected; the user design still functions, but the external configuration controller no longer has visibility or control over the interface with the Virtex-5QV FPGA.
3. This is not a SEFI, but appears to have SEFI type symptoms. A PROGRAM\_B pulse is too intrusive and all that is needed is for the external configuration controller to issue a START command to continue operations.

# *Partial Re-Configuration*

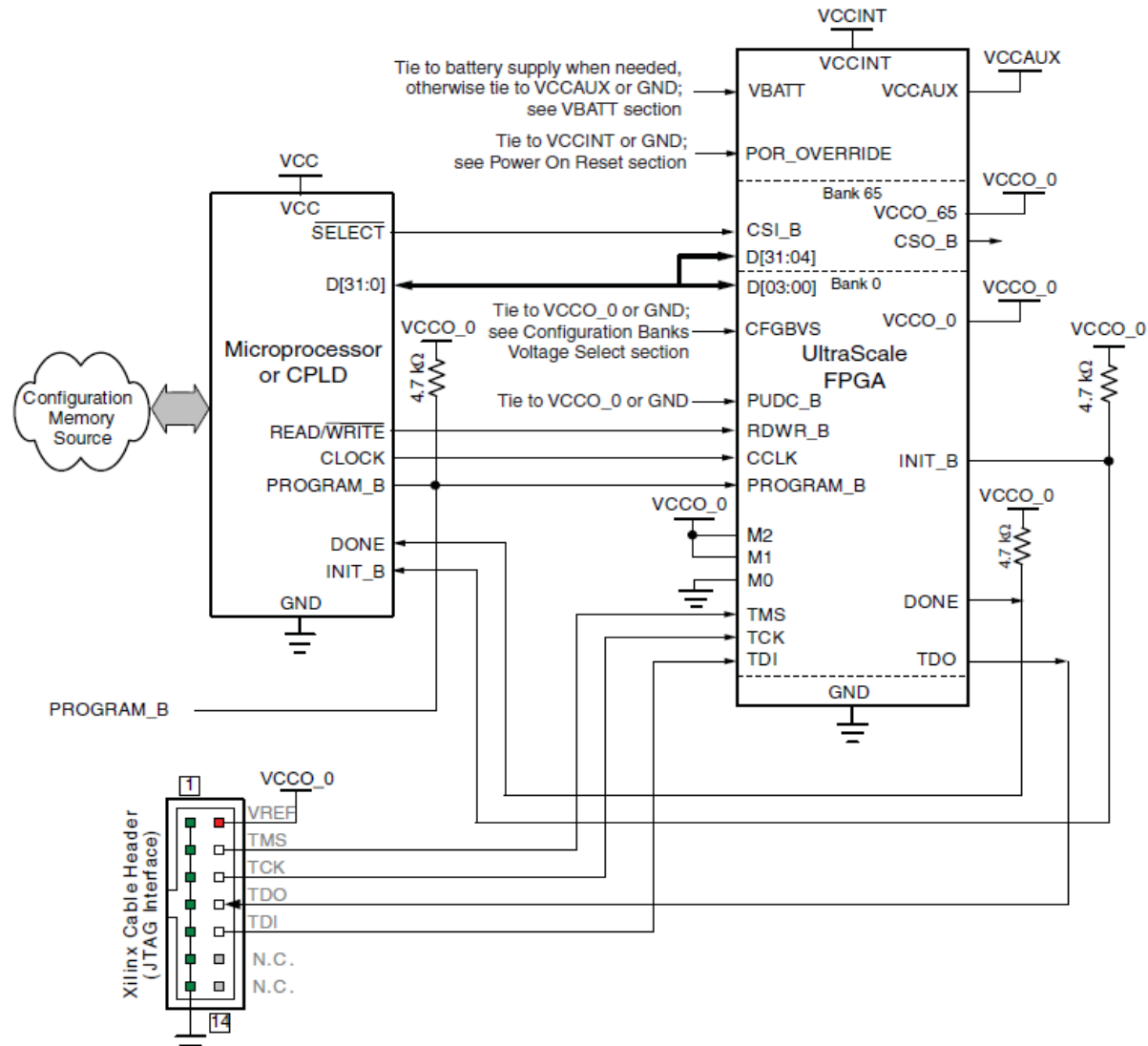




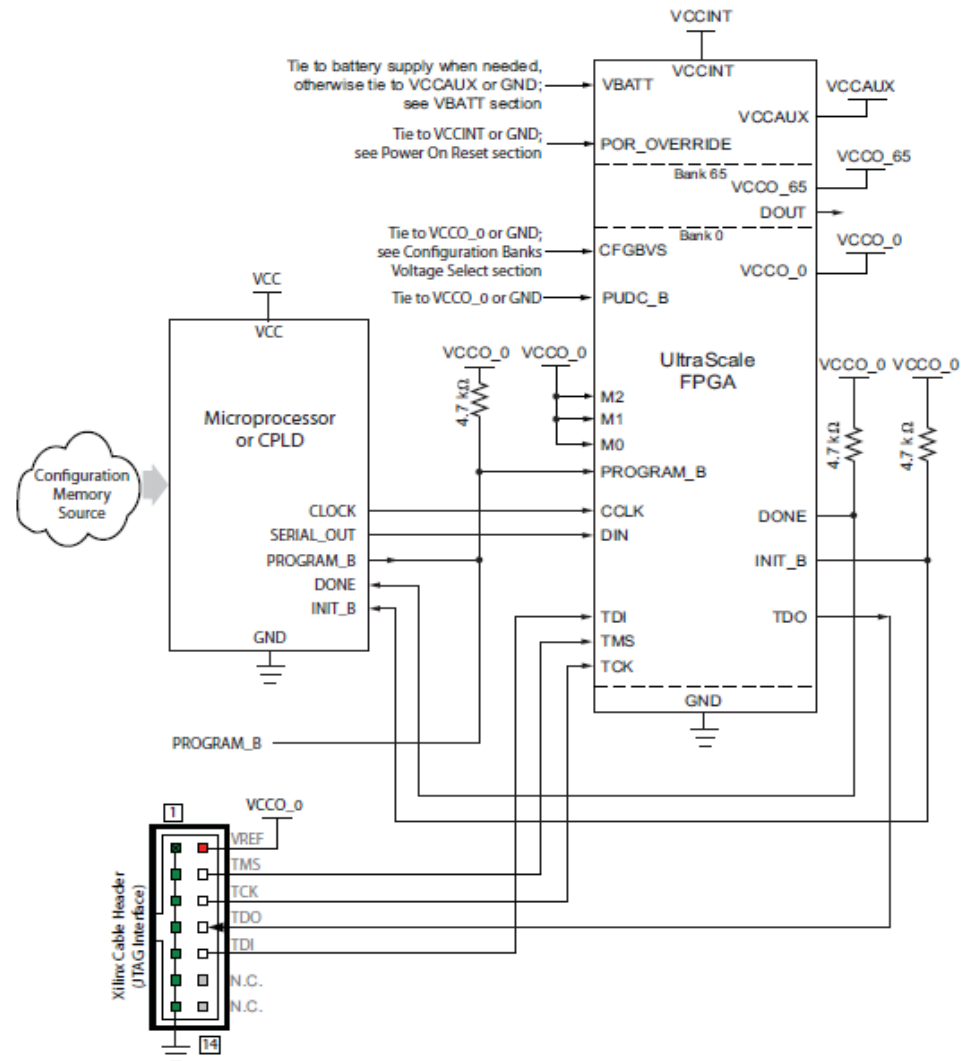
# *Clock rates, data widths and bandwidths for XQRKU060 configuration ports*

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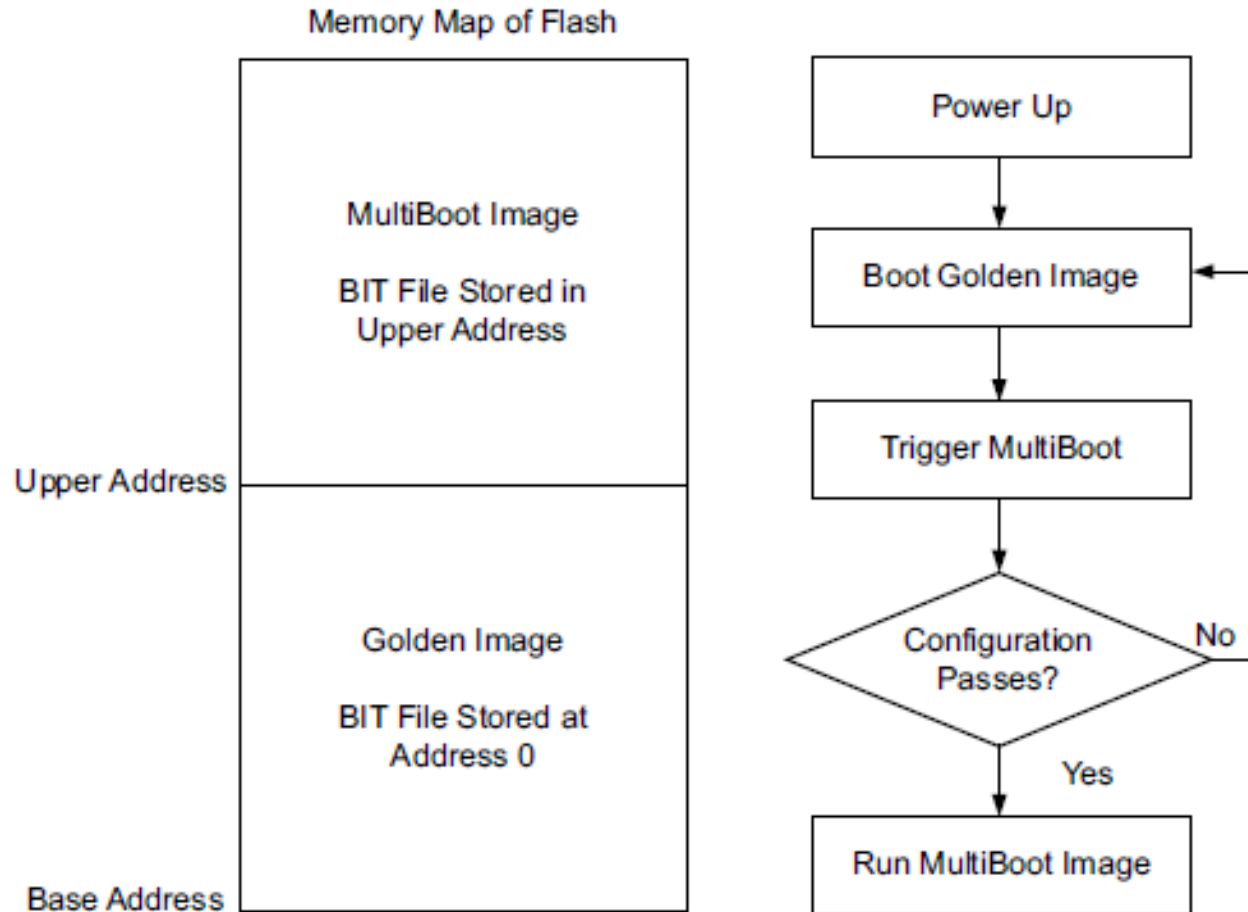
# Slave SelectMap Configuration Mode



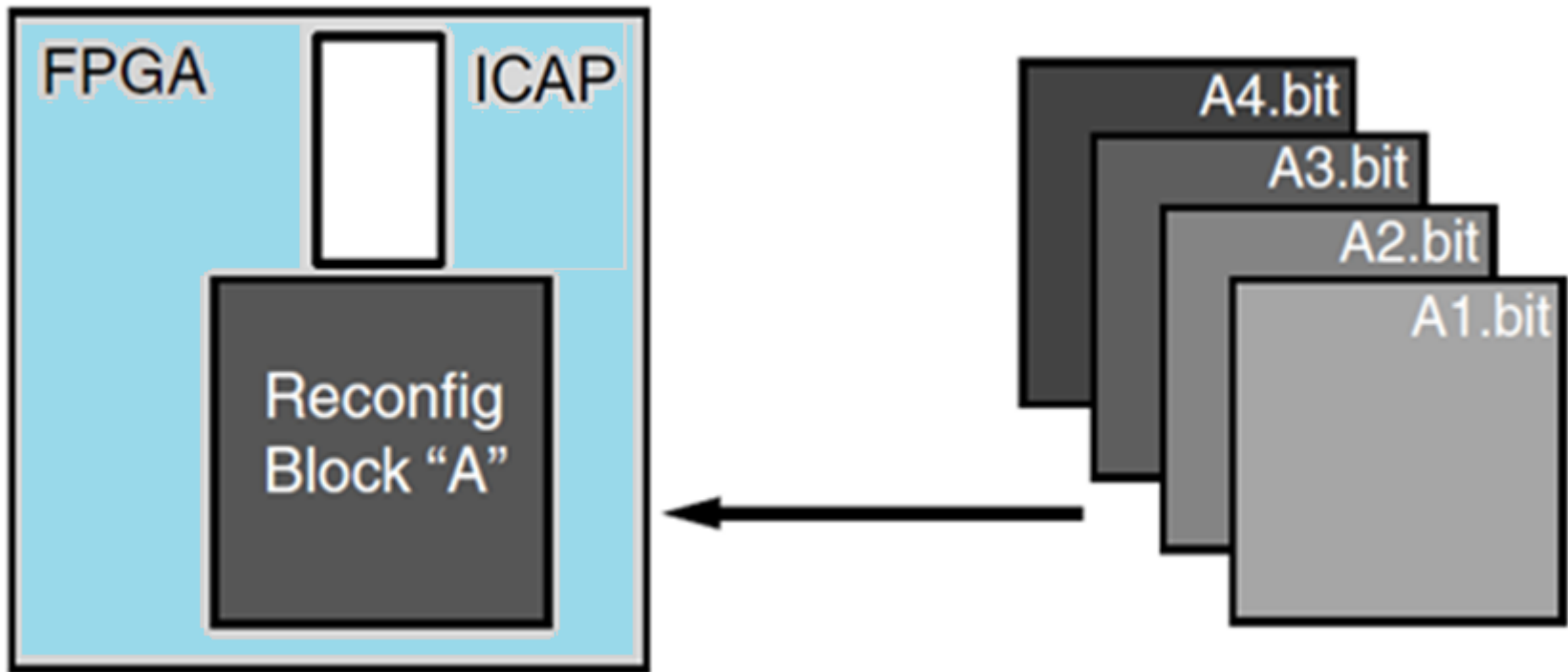
# Slave Serial Configuration Mode



# *MultiBoot to Select Multiple Bitstreams*



# *Partial Re-Configuration*



# Conclusions

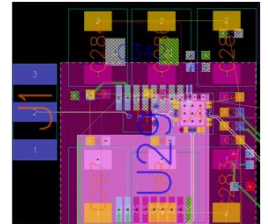
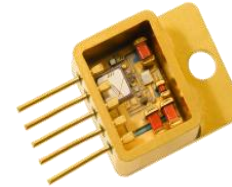
- *XQRKU060 offers Internal & External Scrubbing Options*
  - *Internal Readback and Writeback via SEM IP*
  - *External Blind Scrubbing with Readback/Writeback*
  - *External Blind Scrubbing without Readback*
- *XQRKU060 offers In-Orbit Re-Configuration Options*
  - *Slave Serial SelectMap port can be accessed after configuration to access external SPI flash*
  - *Multiboot stores multiple bitstreams in external flash memory*
  - *Partial Re-Configuration of a single frame or the complete bitstream*



- *Products*



- *Design-Consultancy Services*



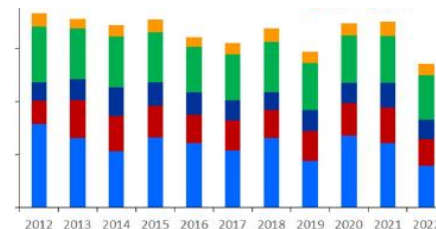
- *Training Services*



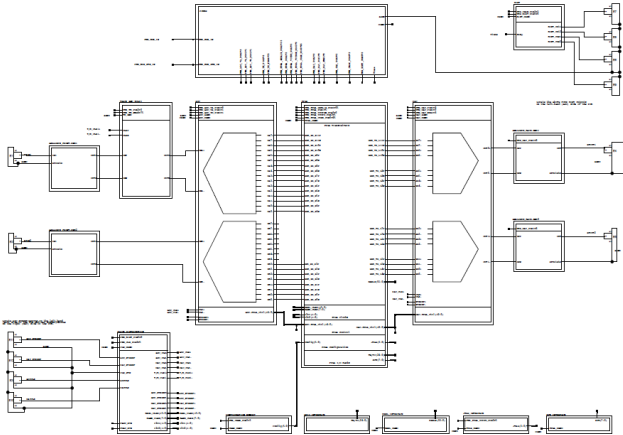
- *Technical-Marketing Services*



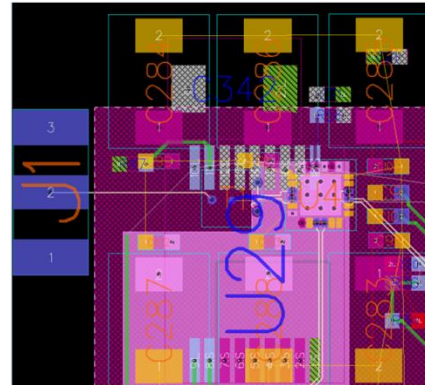
- *Business-Intelligence*



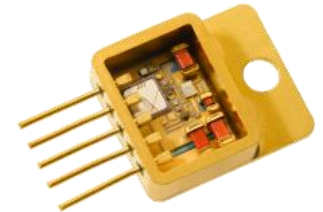
# Design-Consultancy Services



*Schematic Capture*

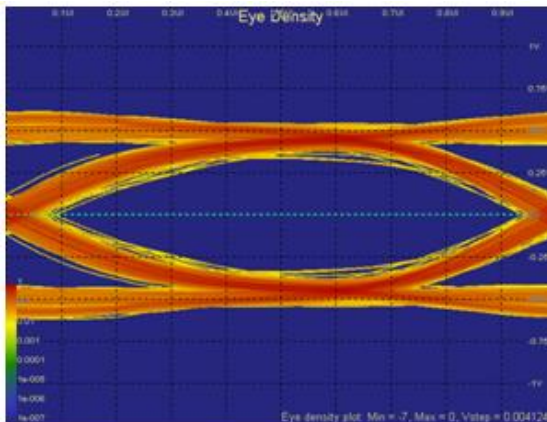


*PCB Layout*

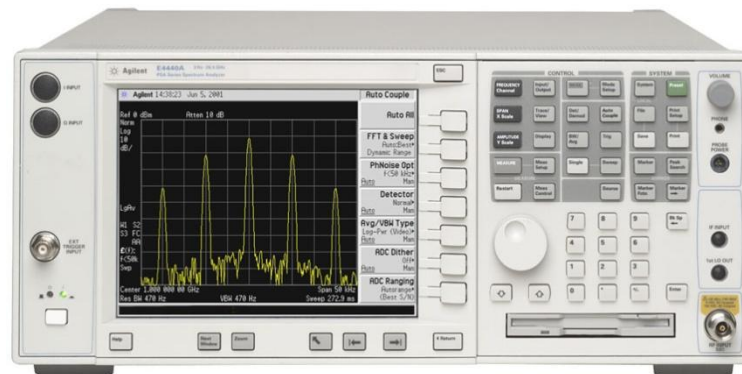


*Parts Selection*

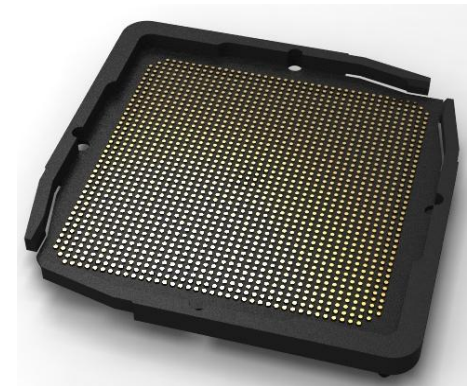
*Reusable, design flow to develop low-cost, satellite electronics right-first-time!*



*Simulation/Analyses*



*Test*

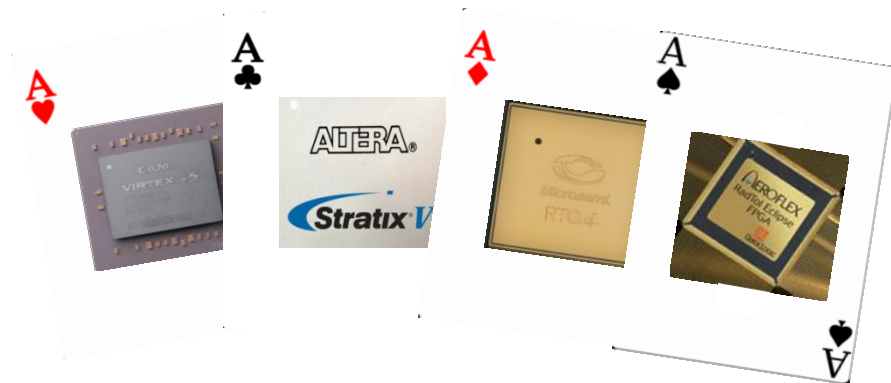


*Assembly & Manufacture*

# *Training Courses on Space Electronics*



- *Help companies/countries develop local expertise and capability to become self-sufficient.*
- *Help companies develop Space Electronics right-first-time, to cost and schedule, preventing over-engineering, delivering late and spending too much.*
- *Courses teach and compare all space-grade electronic components including low-cost COTS parts.*
- *Courses are unique and not offered by anyone else in the world.*
- *Each attendee receives a personal copy of all 900 slides.*





# 600 Space Professionals in 13 Countries



Class of Tel Aviv



Class of Singapore



Class of South Korea



Class of Harwell, UK



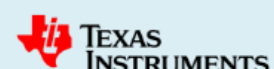
Class of Germany



Class of Turkey

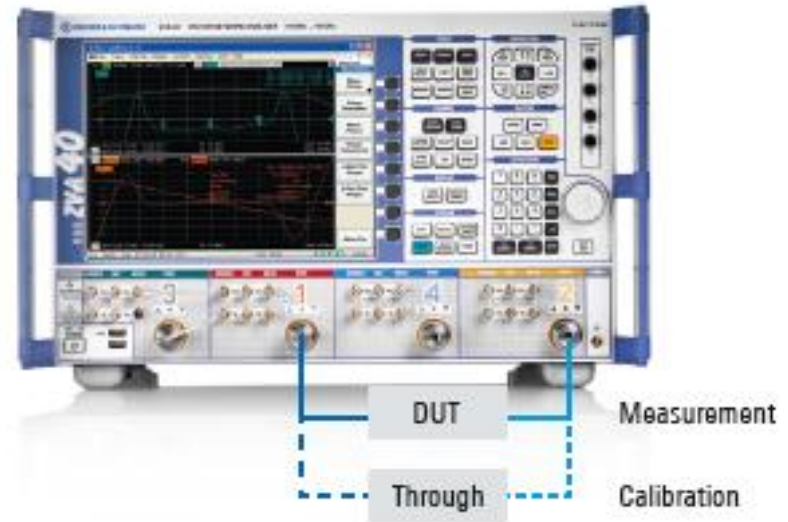


Class of Bremen



# *Training Services*

## **Webinars**



***Satellite Payload Testing***

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**Free monthly articles on Space Electronics including  
FPGAs, power, radiation effects, test & EDA**

**Will be publishing articles on Scrubbing & In-Orbit Re-Configuration**



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